

FIG. 1

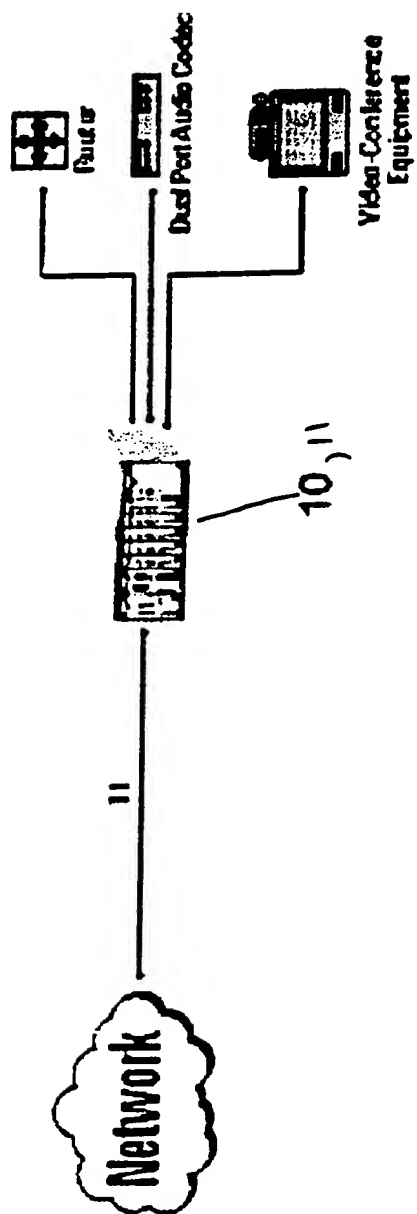


FIG. 2

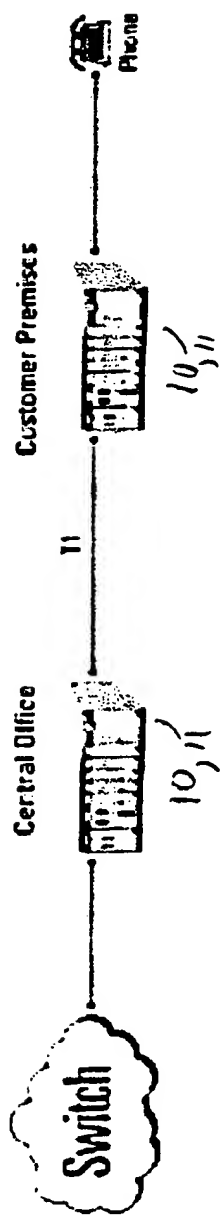


FIG. 4(a)

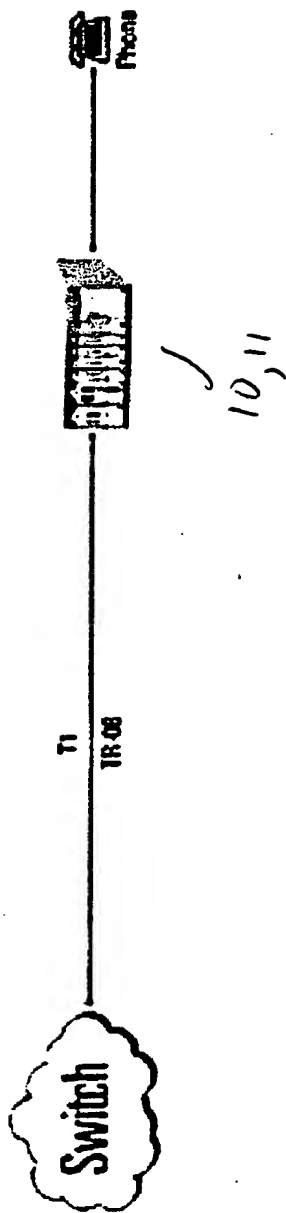


FIG. 4(b)



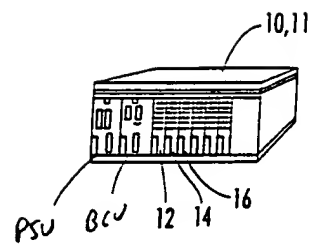


FIG. 5

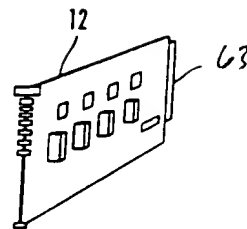


FIG. 6

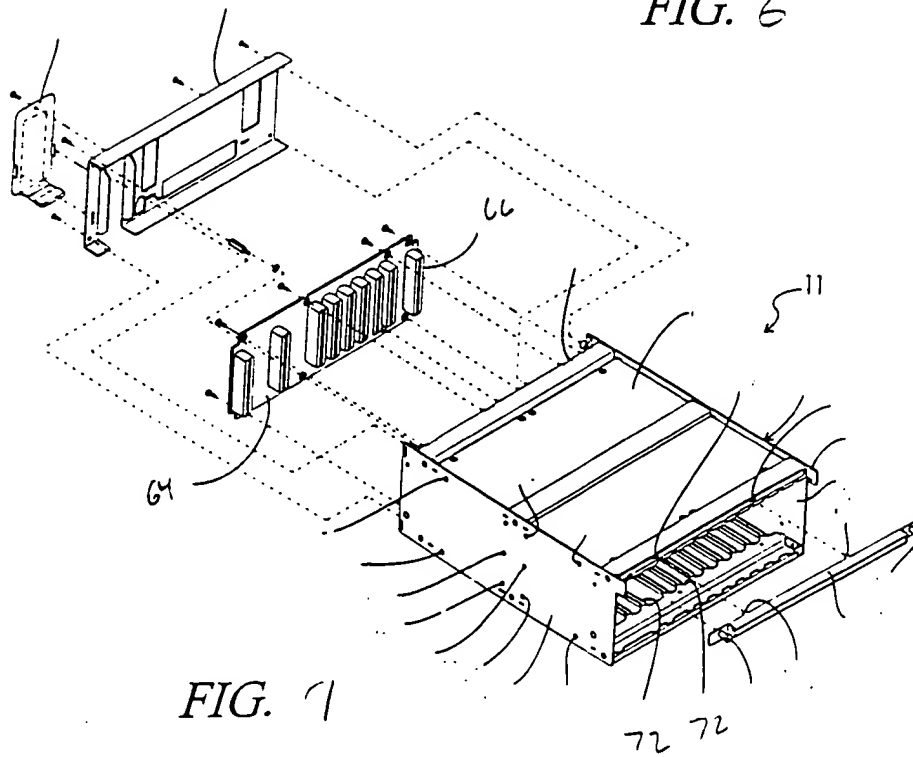


FIG. 7

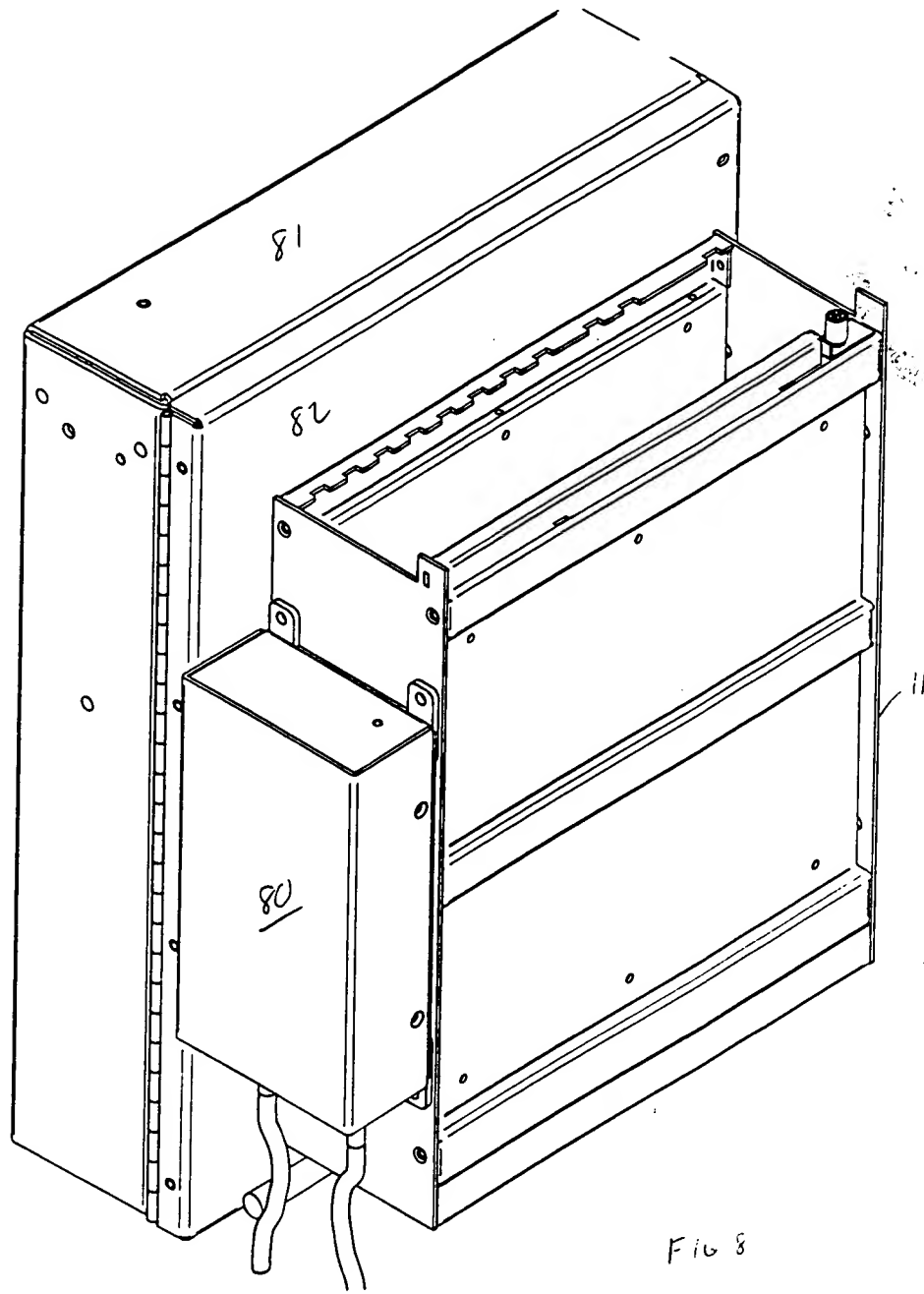
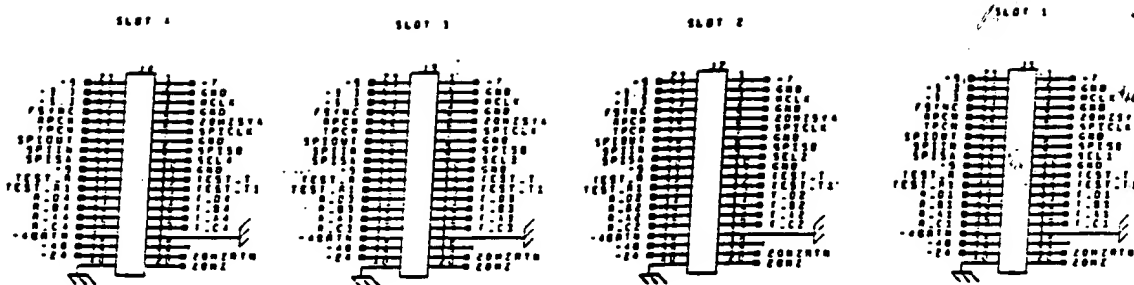


FIG 8





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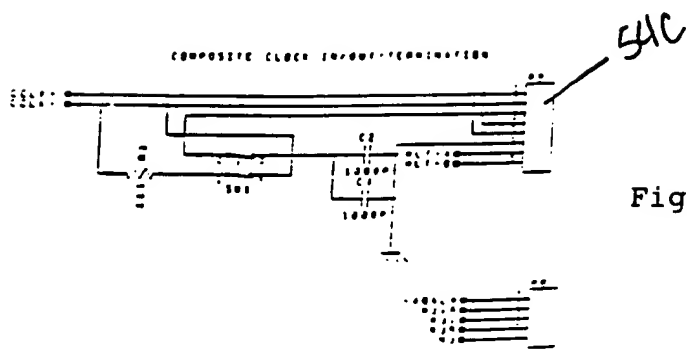
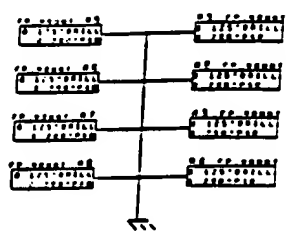
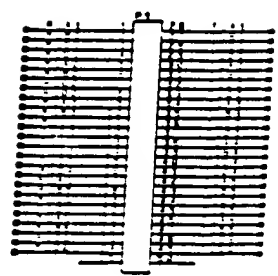


Figure 9 (Continued)

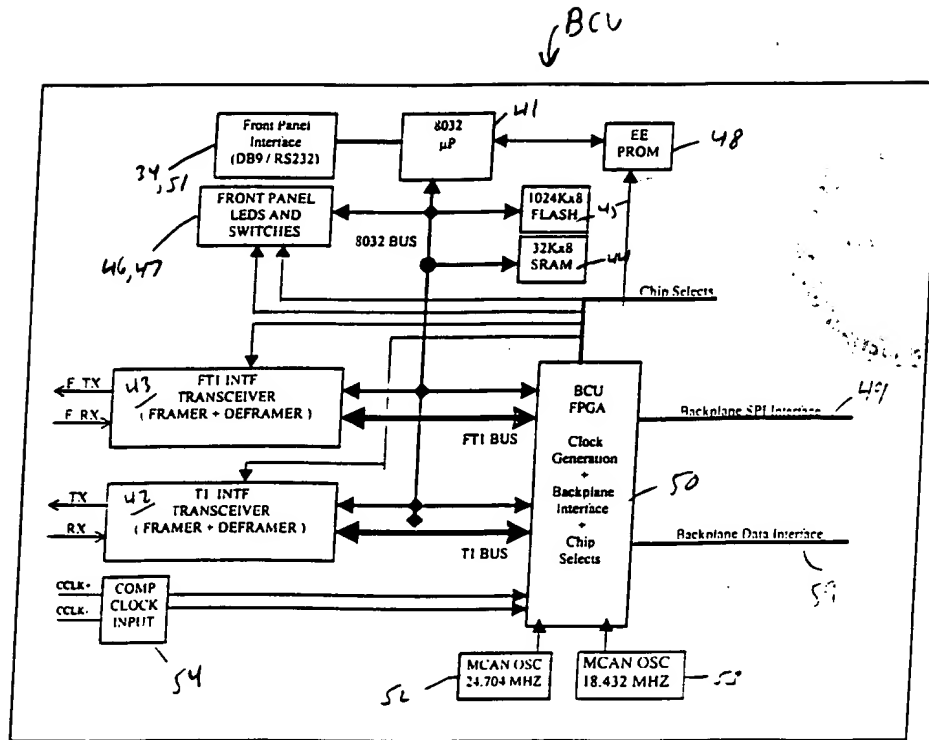
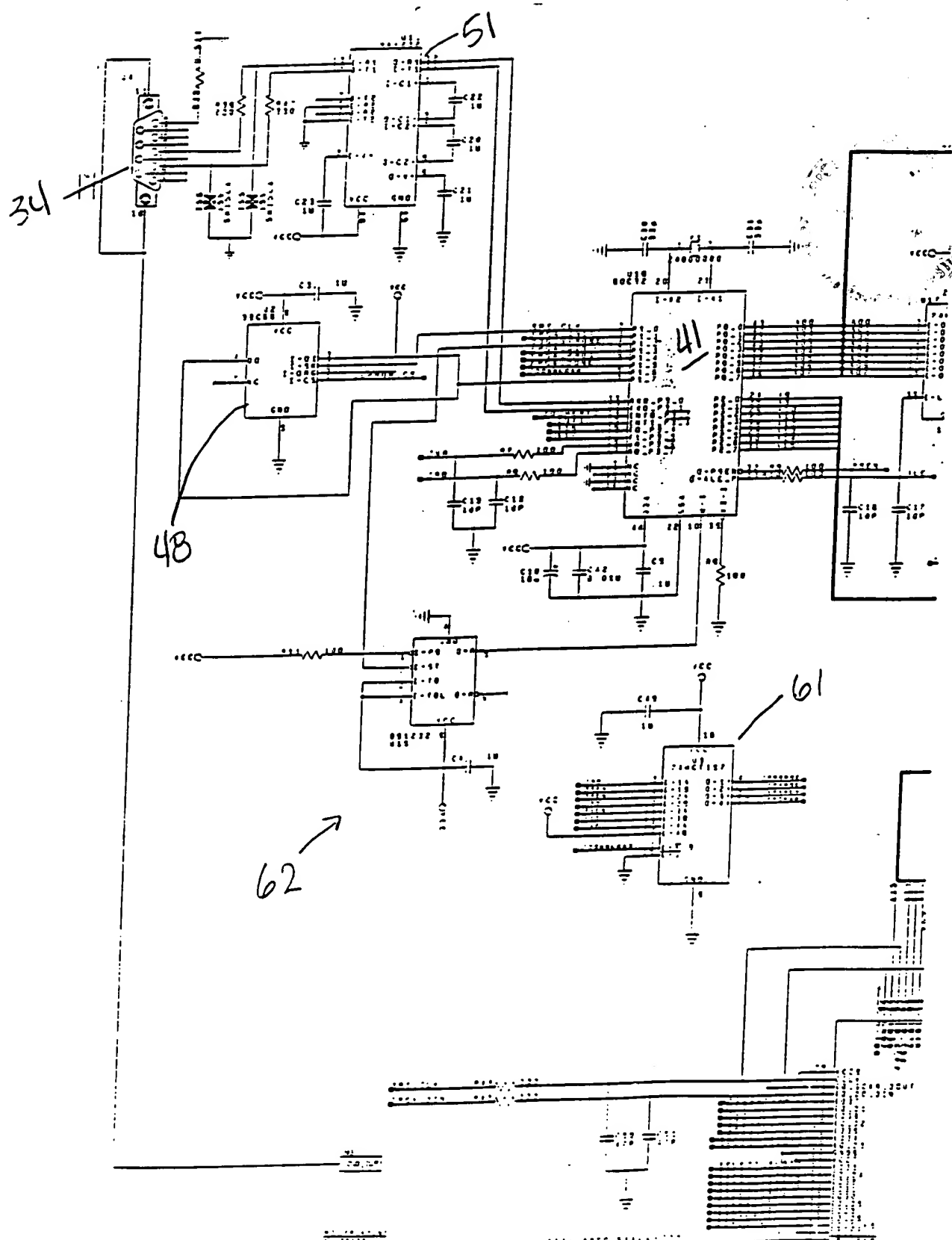


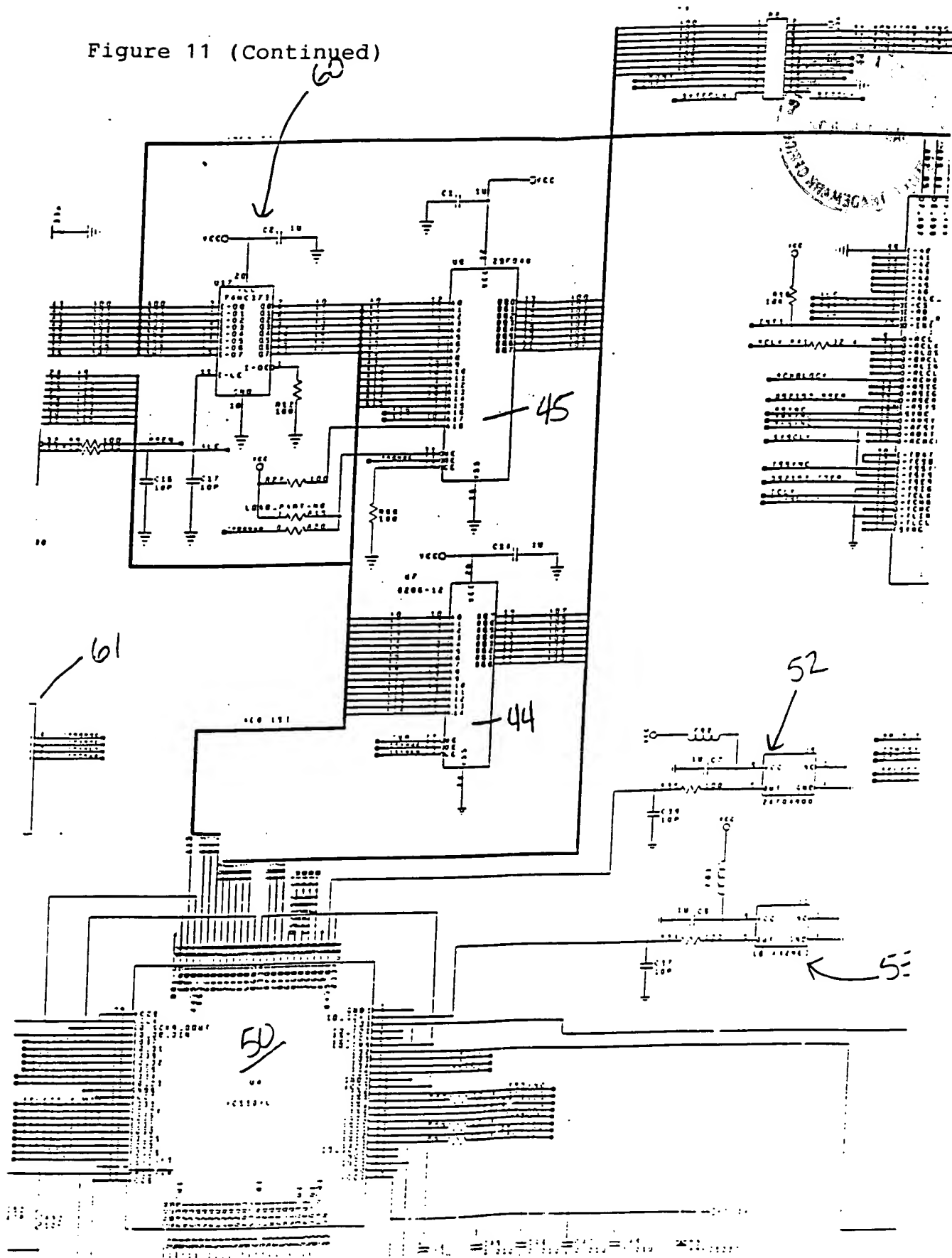
Fig. 10

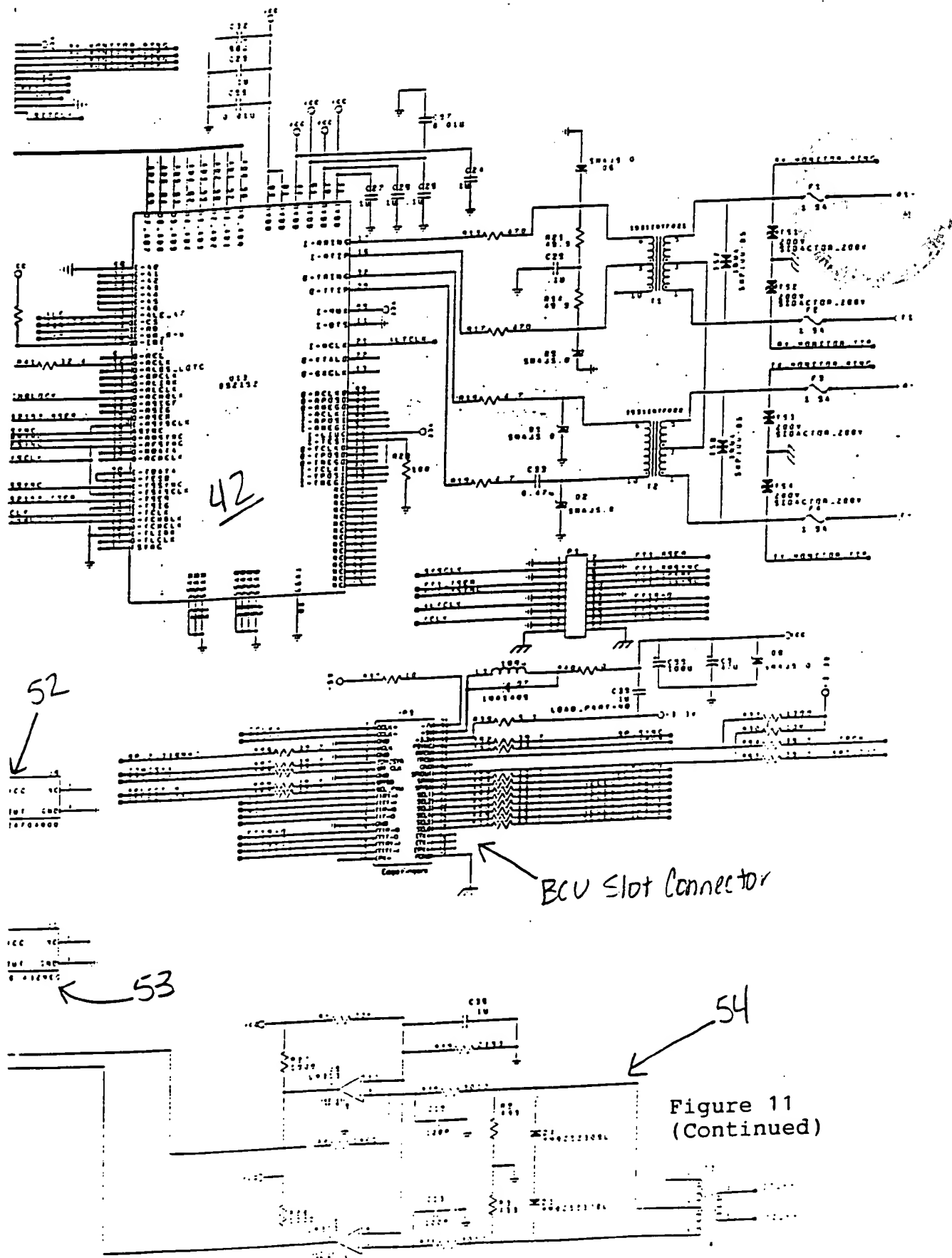




— Figure 11

Figure 11 (Continued)





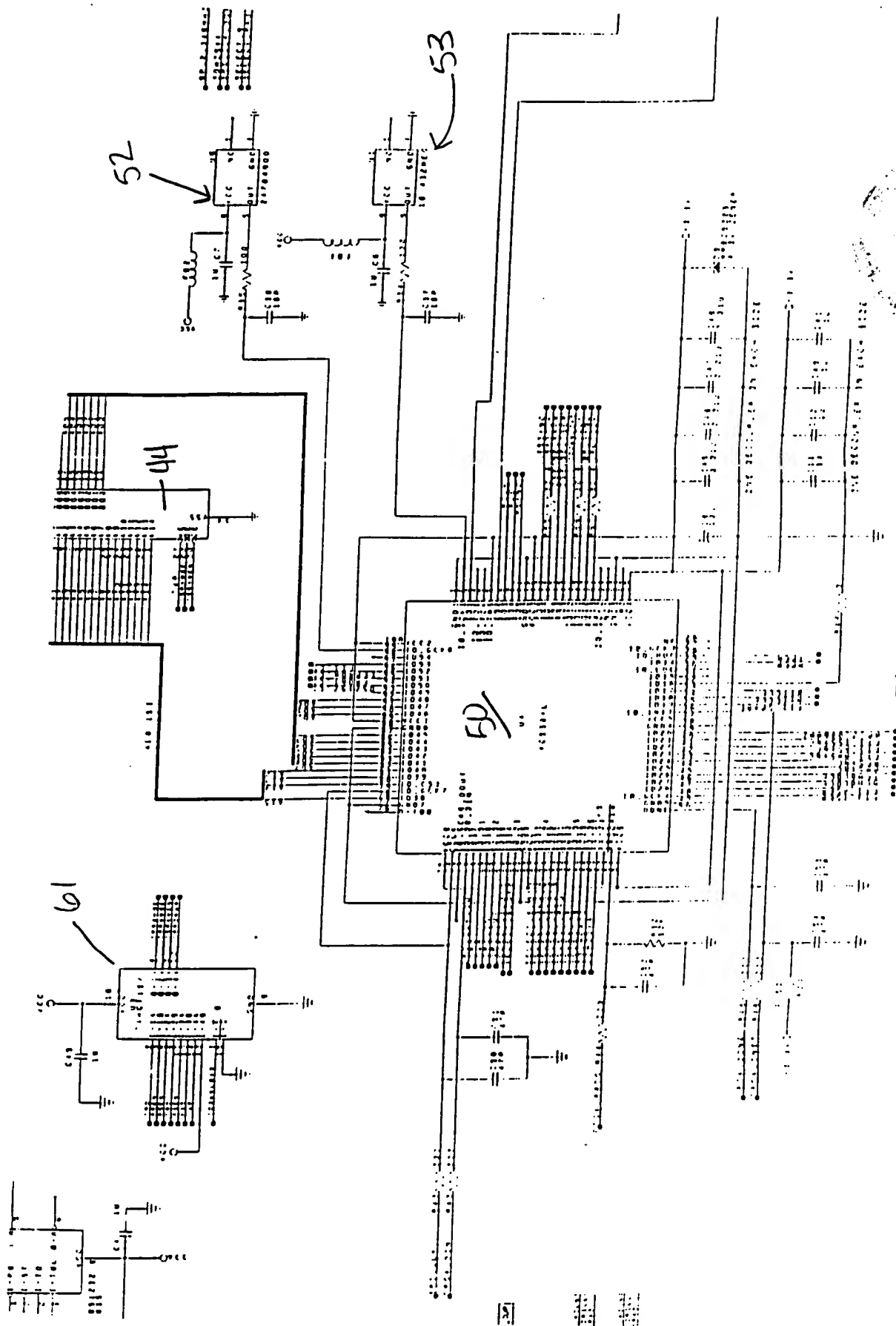


Figure 11 (Continued)

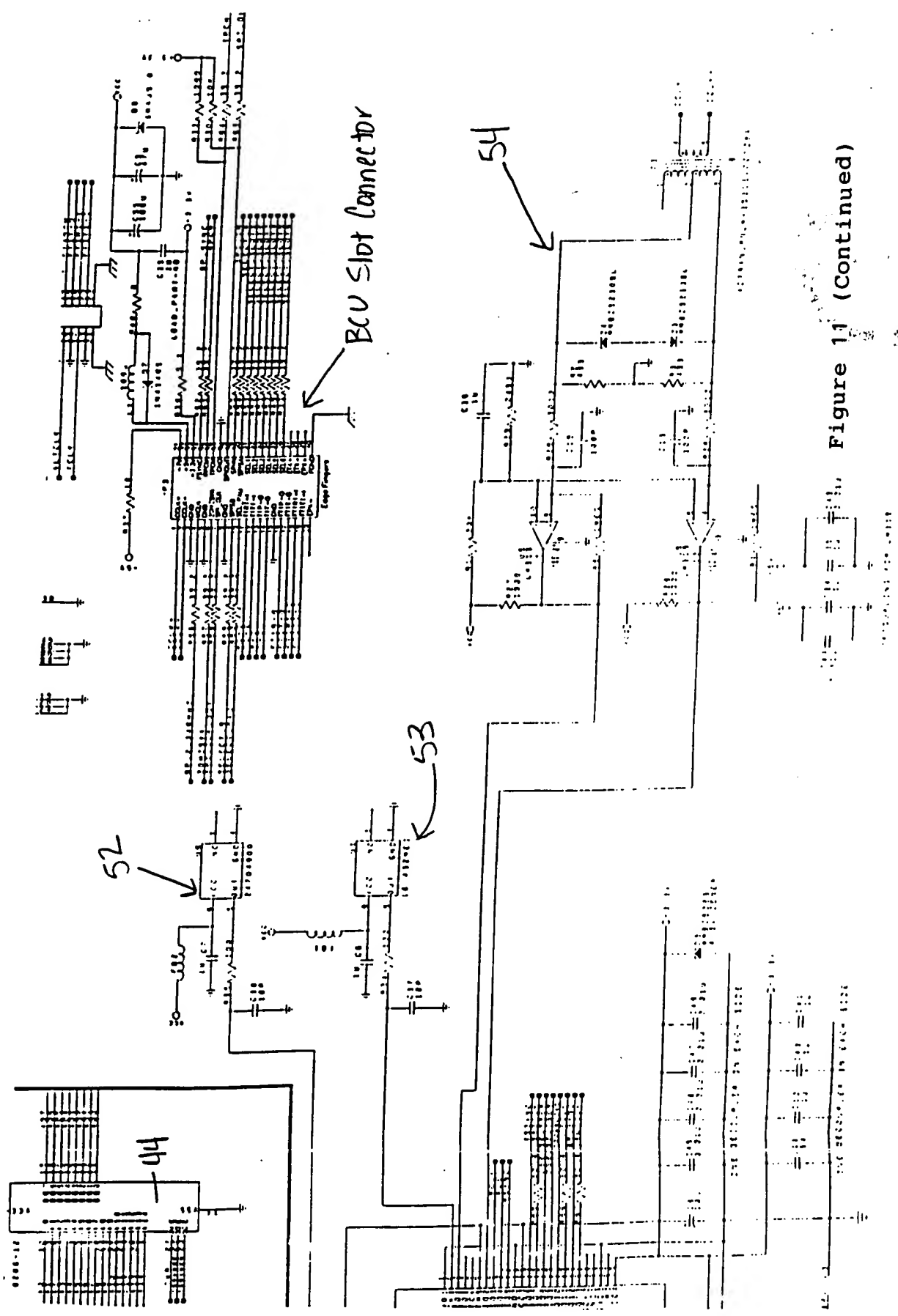
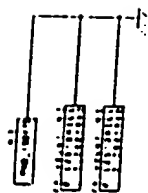


Figure 11 (Continued)



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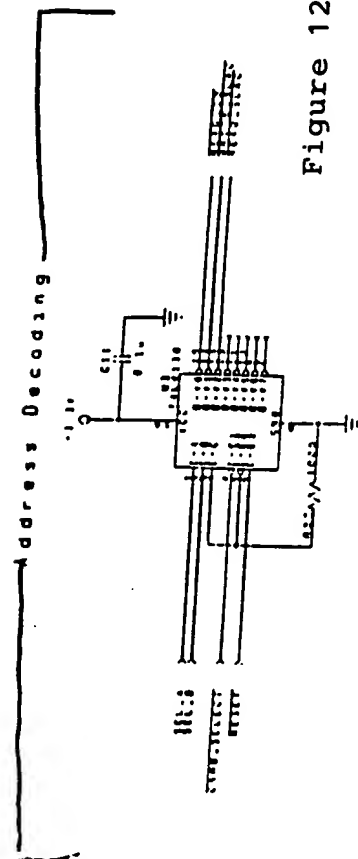
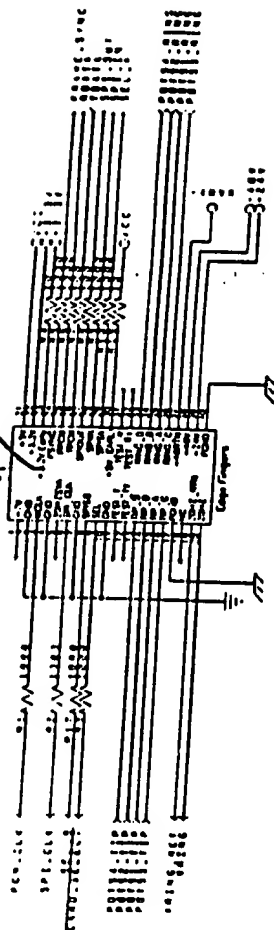
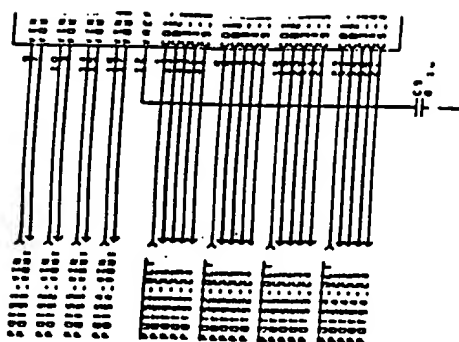
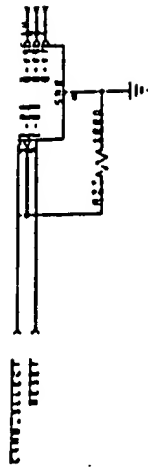


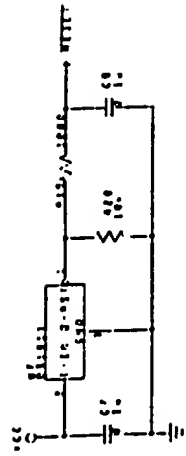
Figure 12 (A)

a.





Power Monitor



Decoupling Capacitors



Interrupt Card

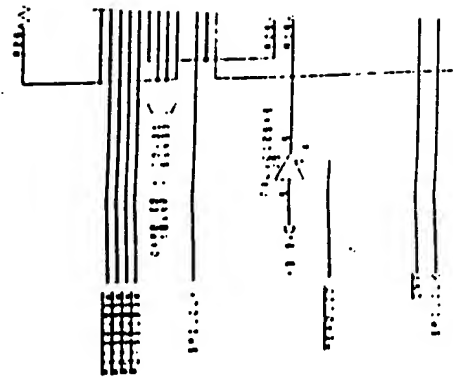


Figure 12(A) (Continued)

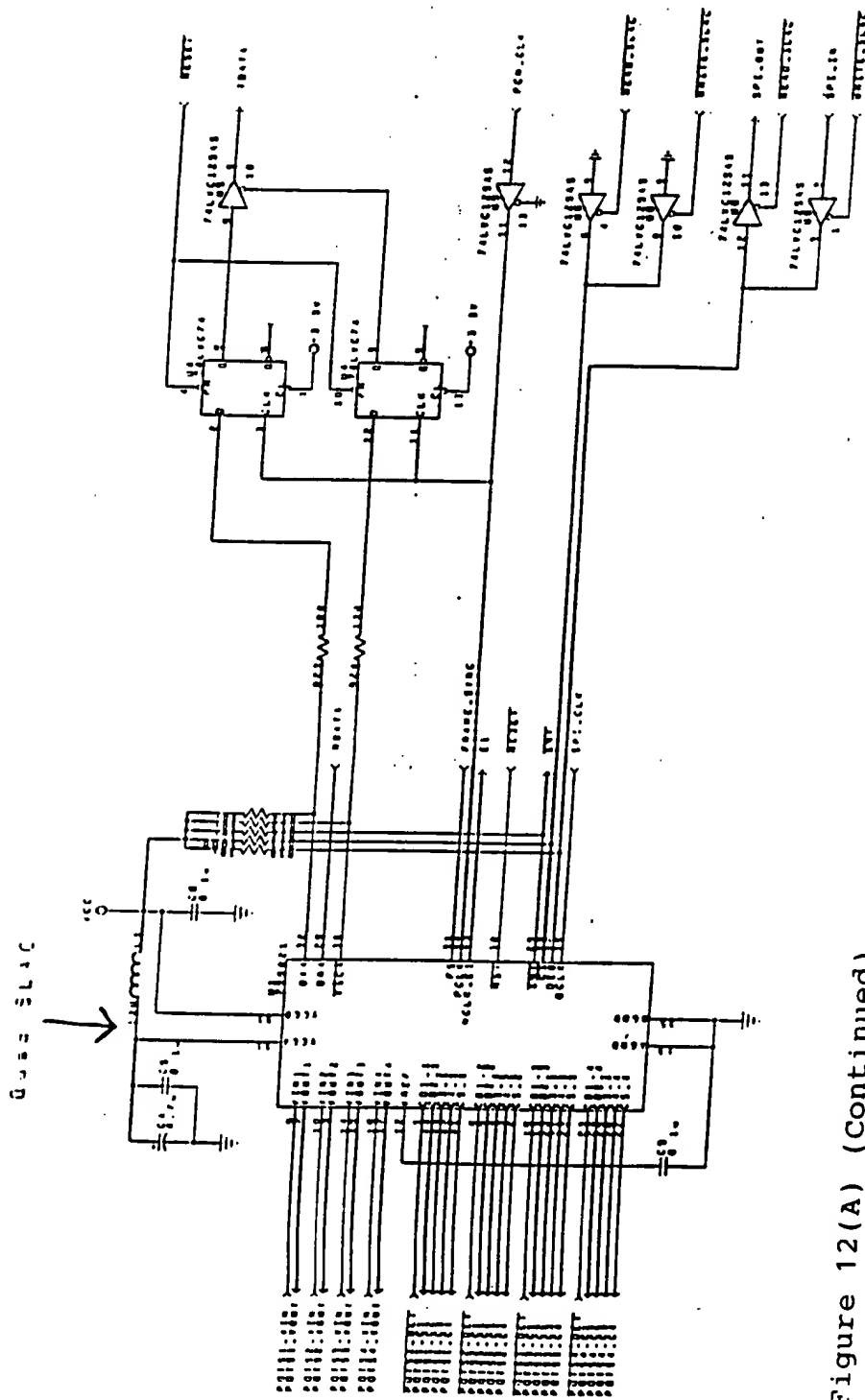


Figure 12(A) (Continued)



Interrupt Card IO and Battery Switch Register

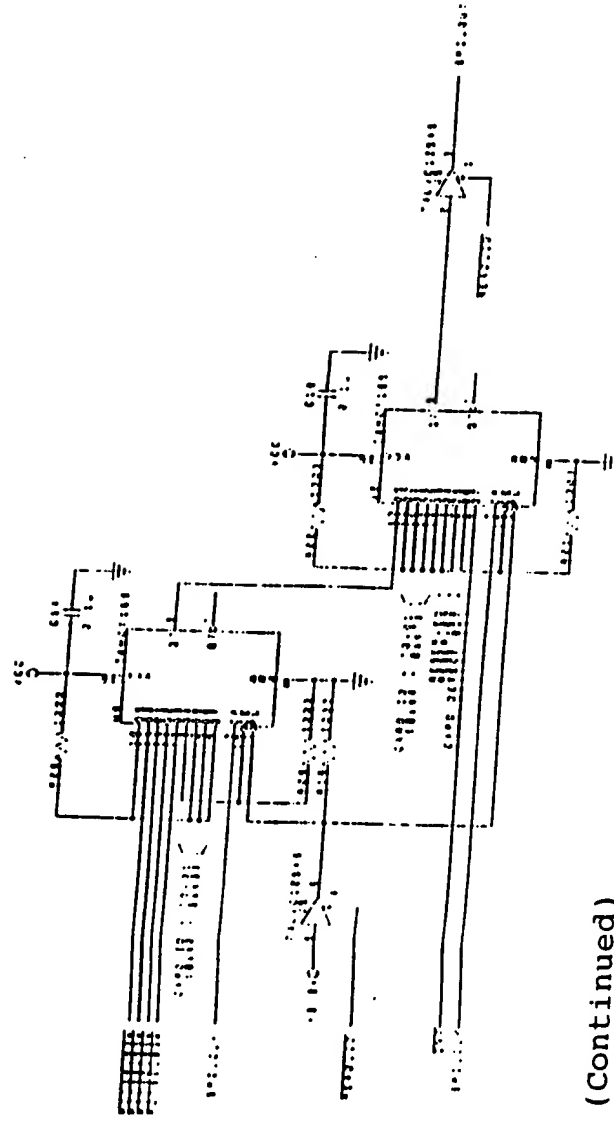


Figure 12(A) (Continued)

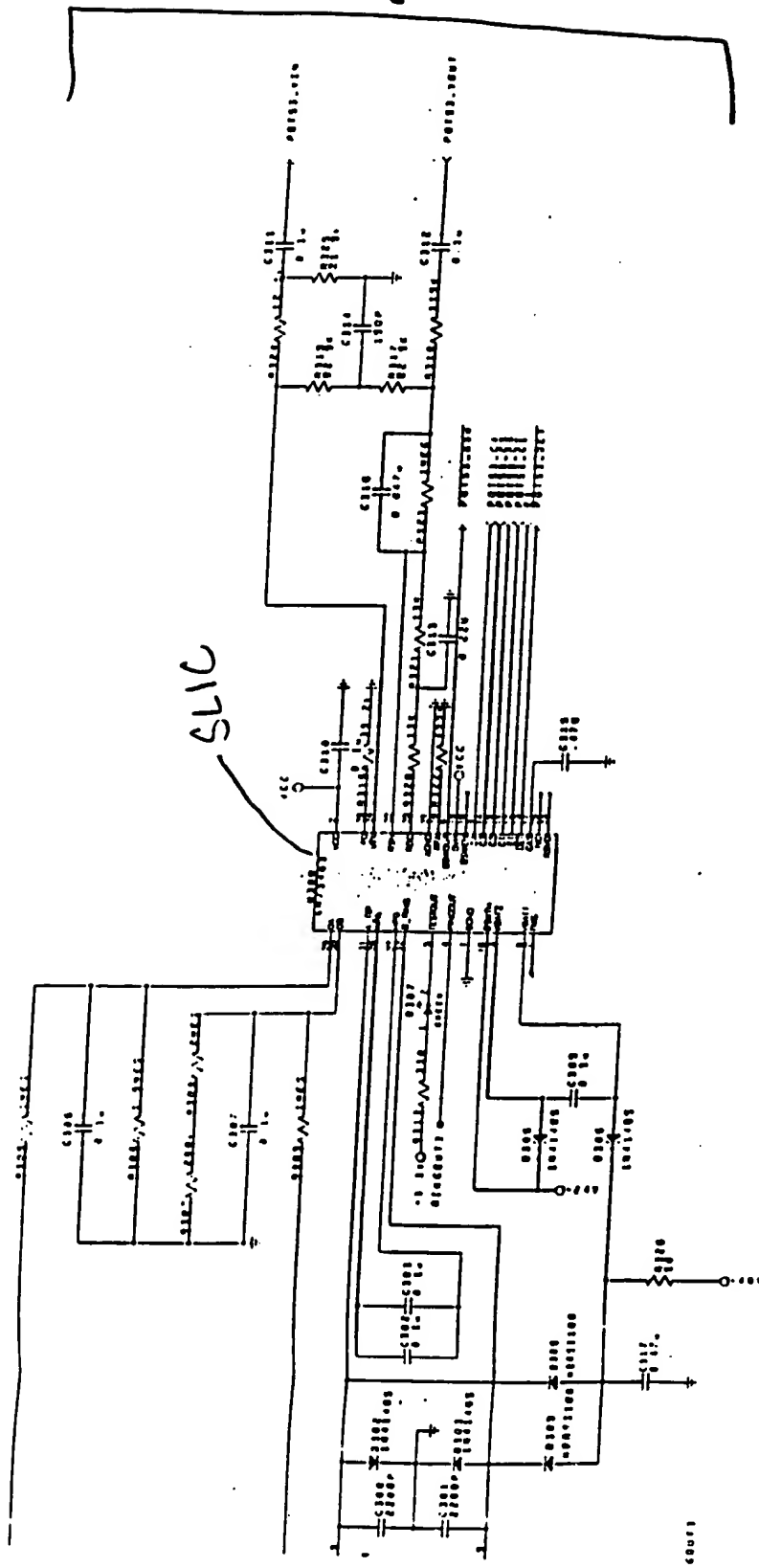
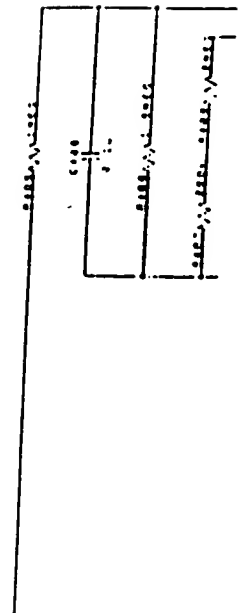


Figure 12(B)



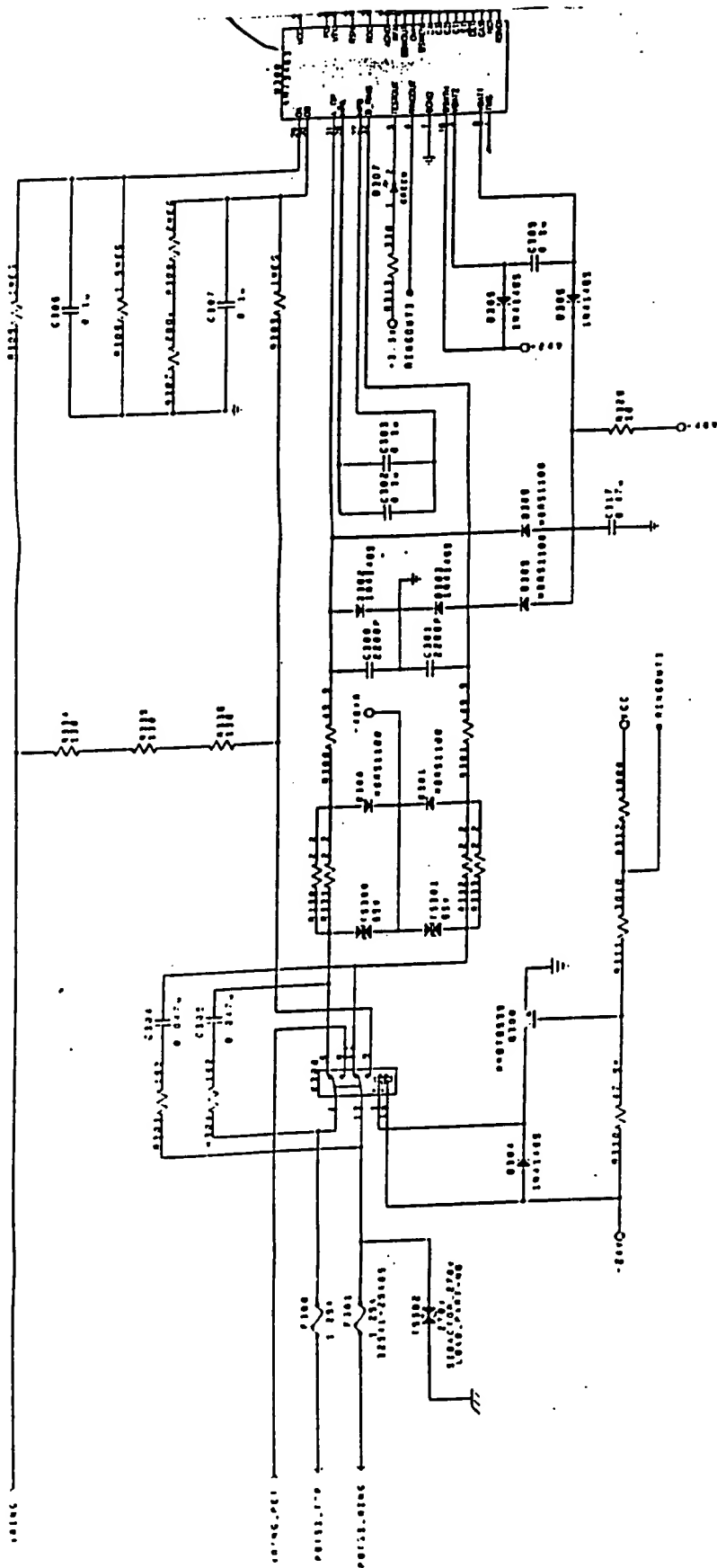


Figure 12(B) (Continued)

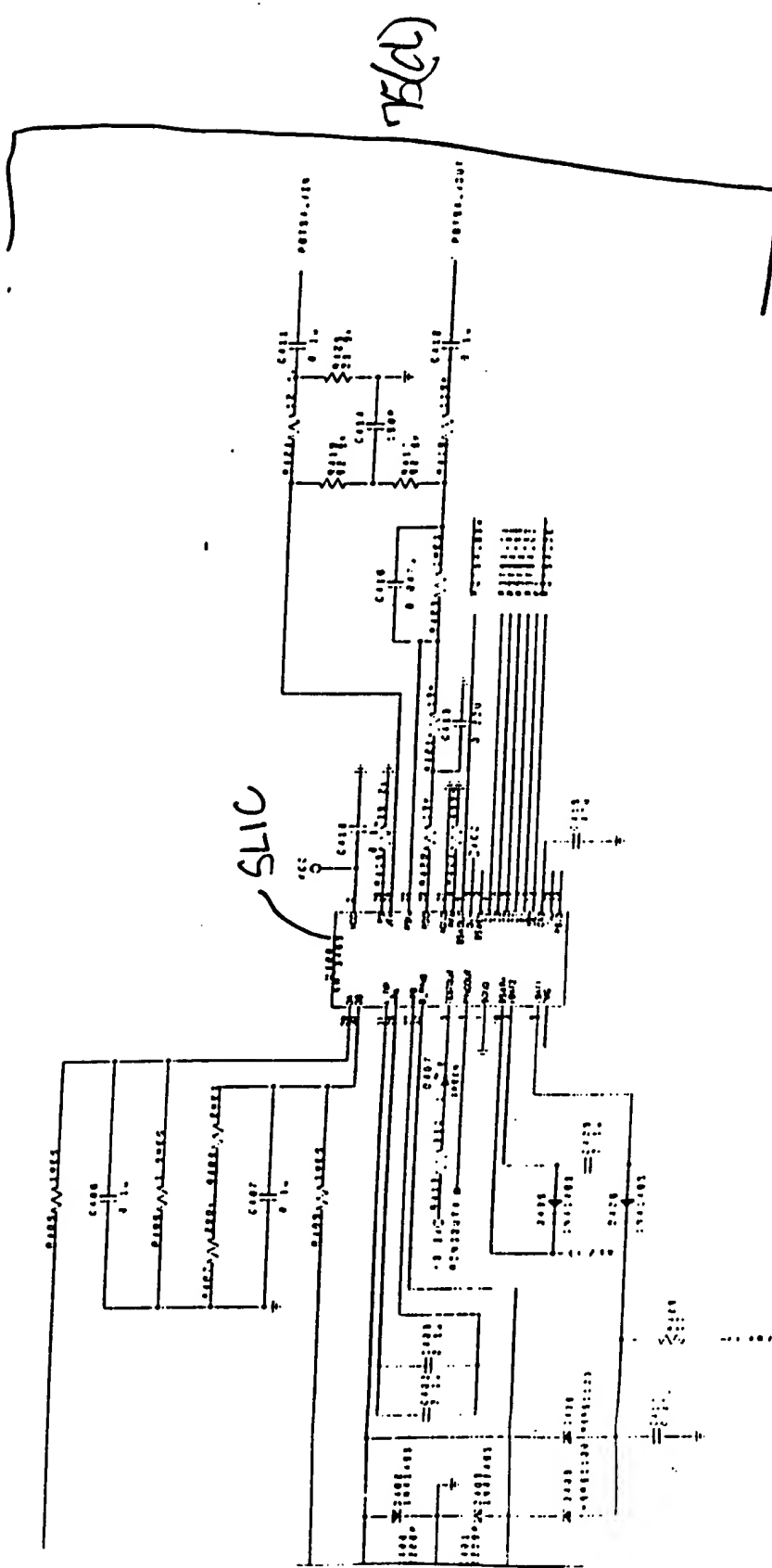


Fig. 12(b)

Figure 12(B) (Continued)

TA 750 Quad POTS RT	2175J08-1
TA 750 Quad POTS RT	2175J08-1
TA 750 Quad POTS RT	2175J08-1
TA 750 Quad POTS RT	2175J08-1

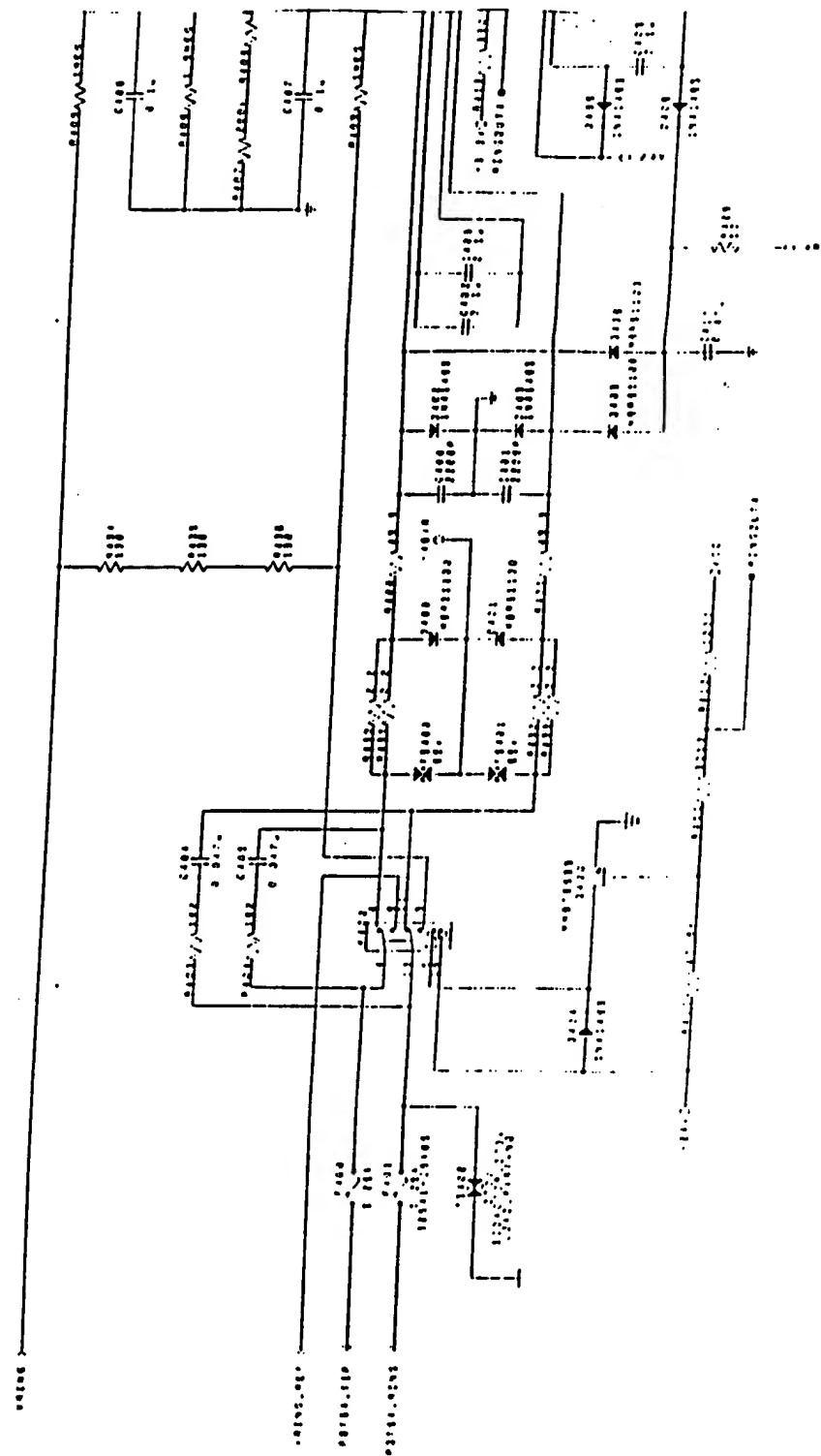
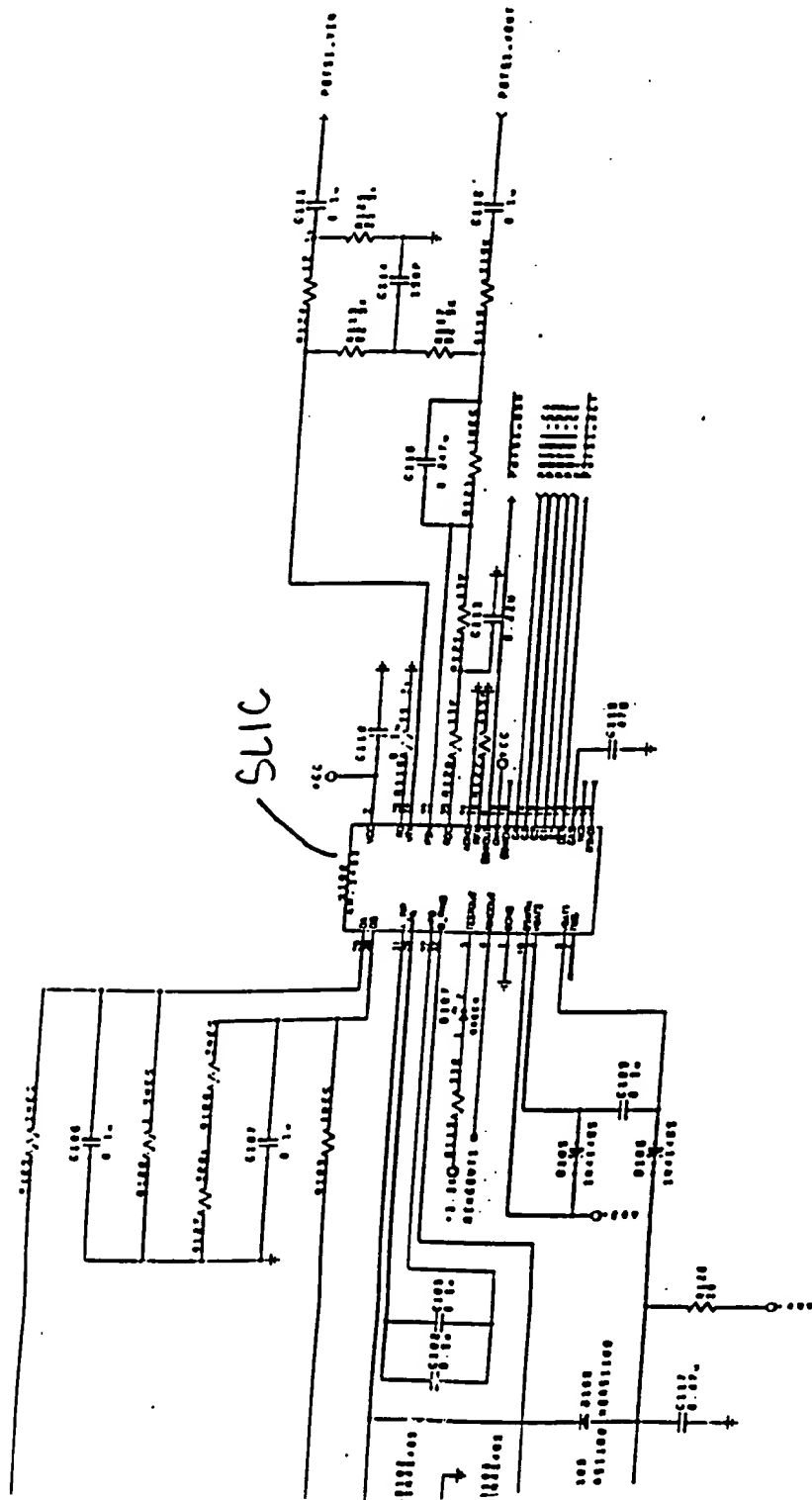


Figure 12(B) (Continued)

Fig. 12(B)



105L

Figure 12(C)

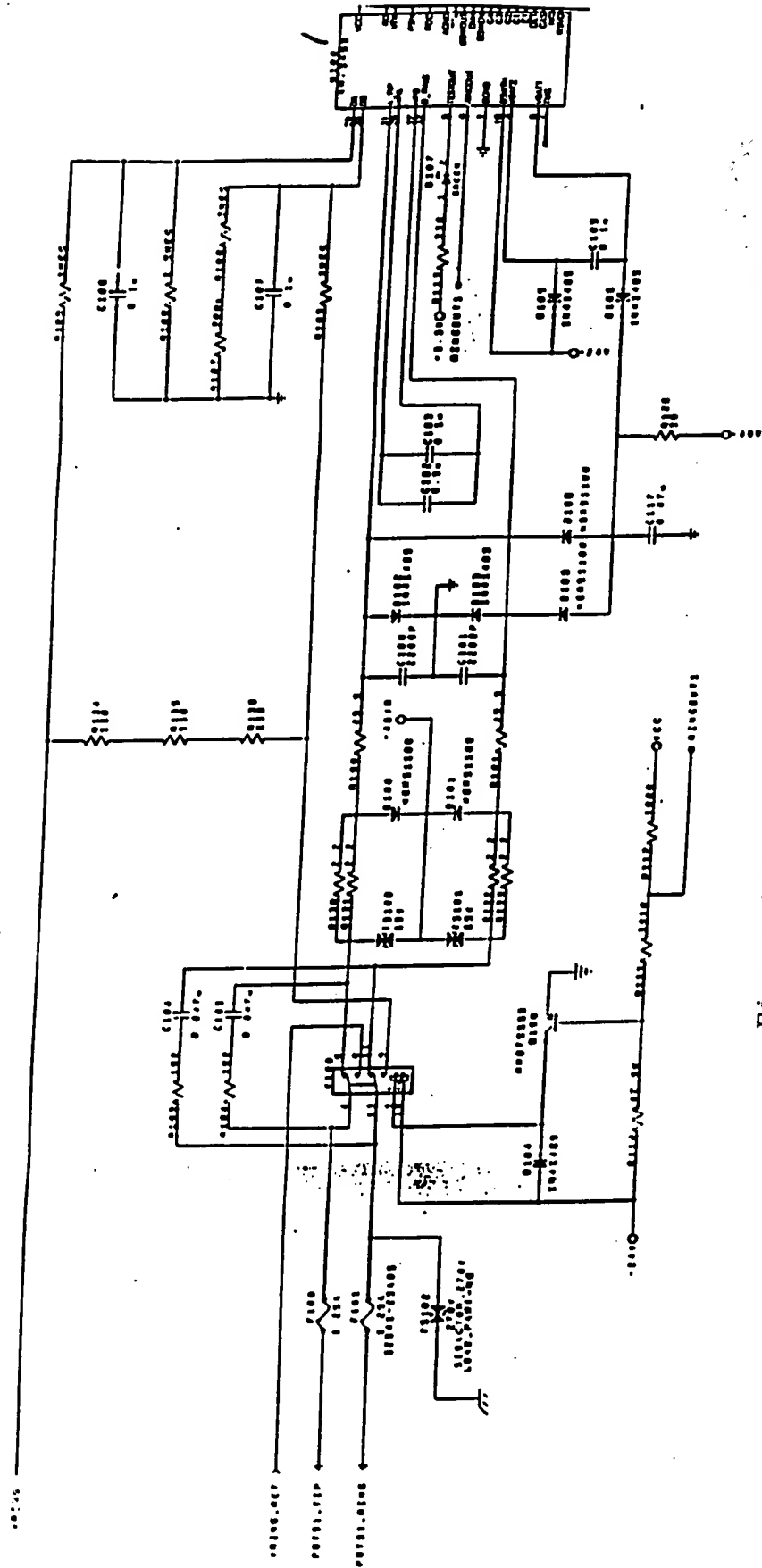


Figure 12(c) (Continued)

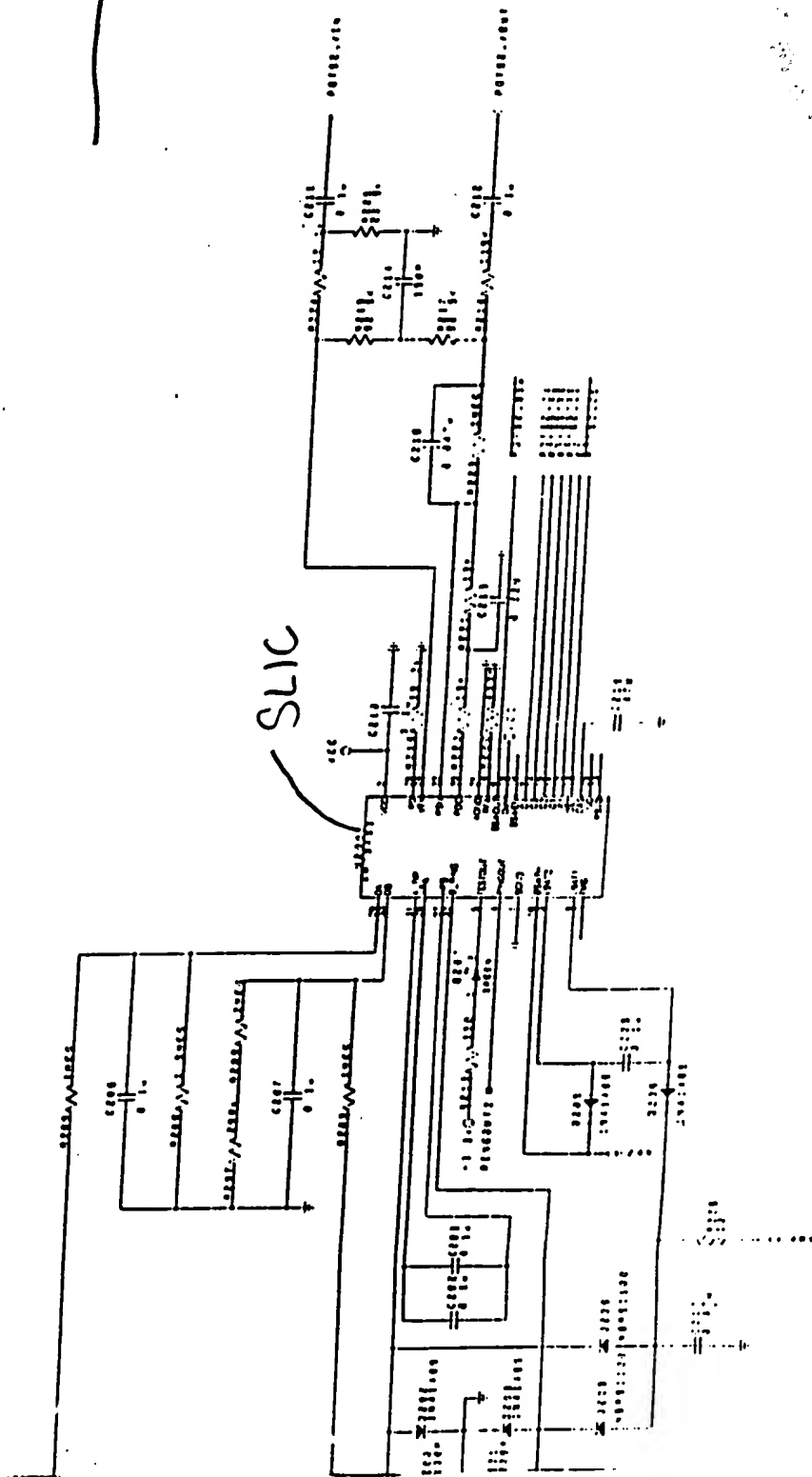


Figure 12(c) (Continued)

15(b)



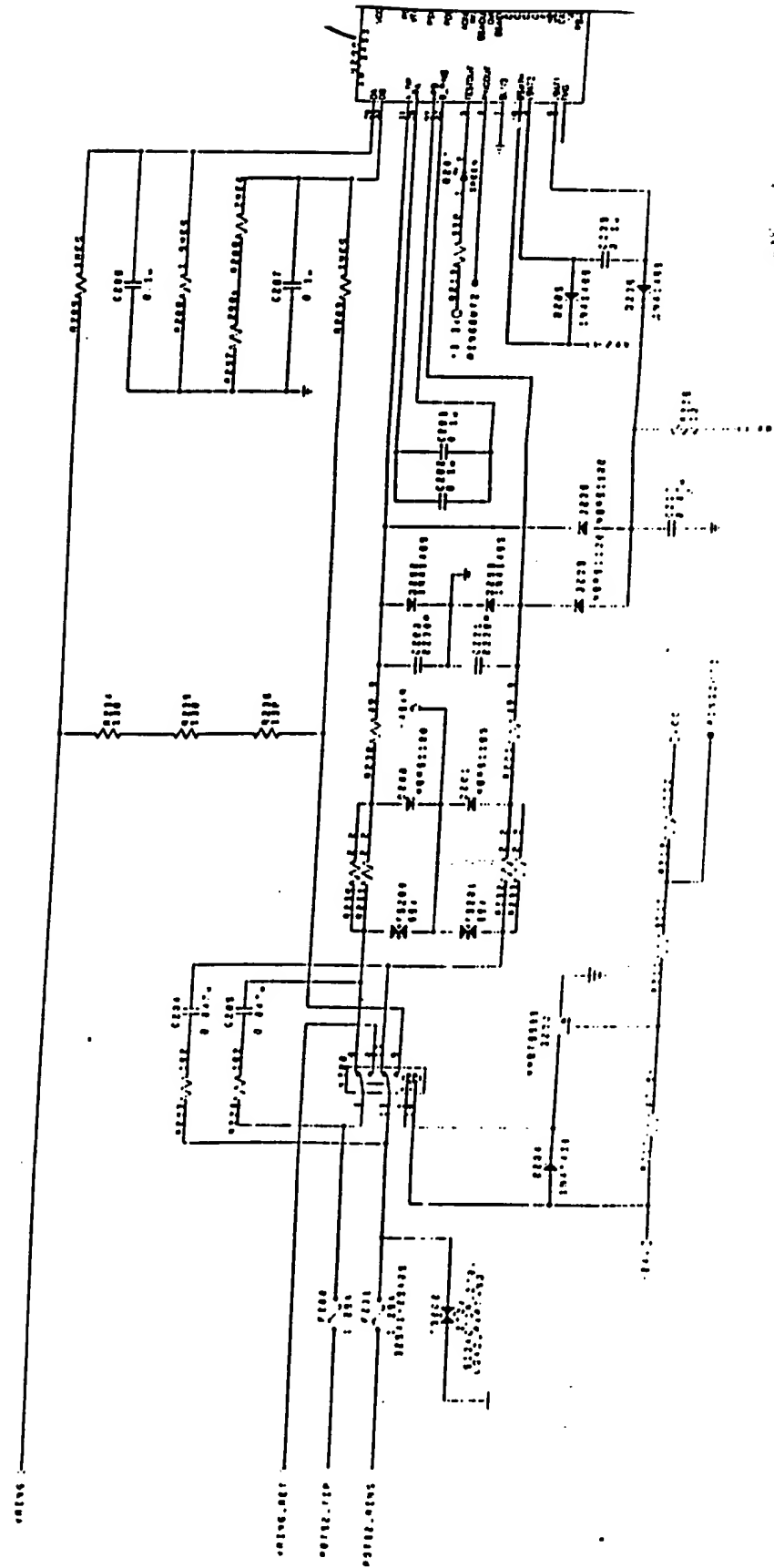
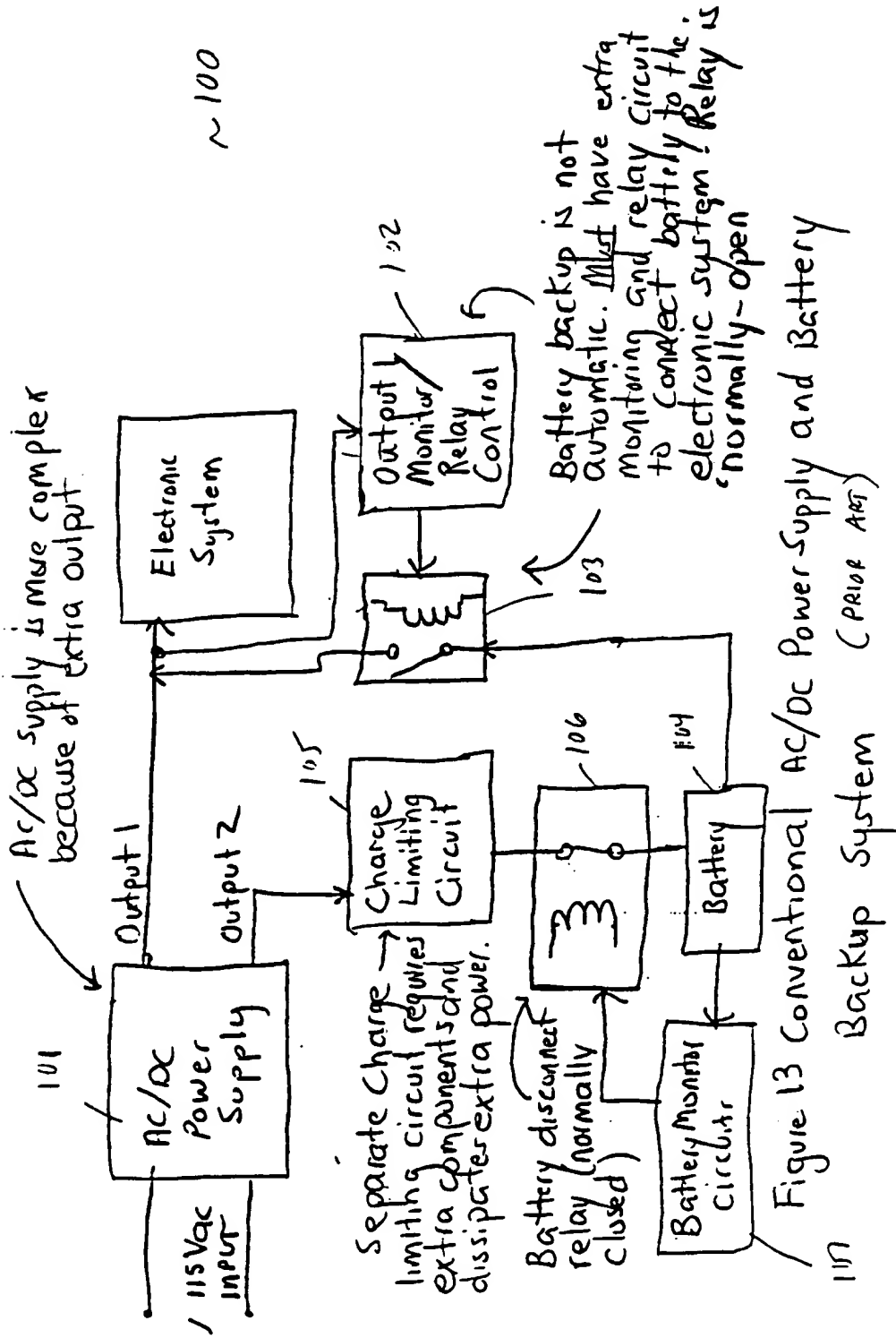


Figure 12(C) (Continued)



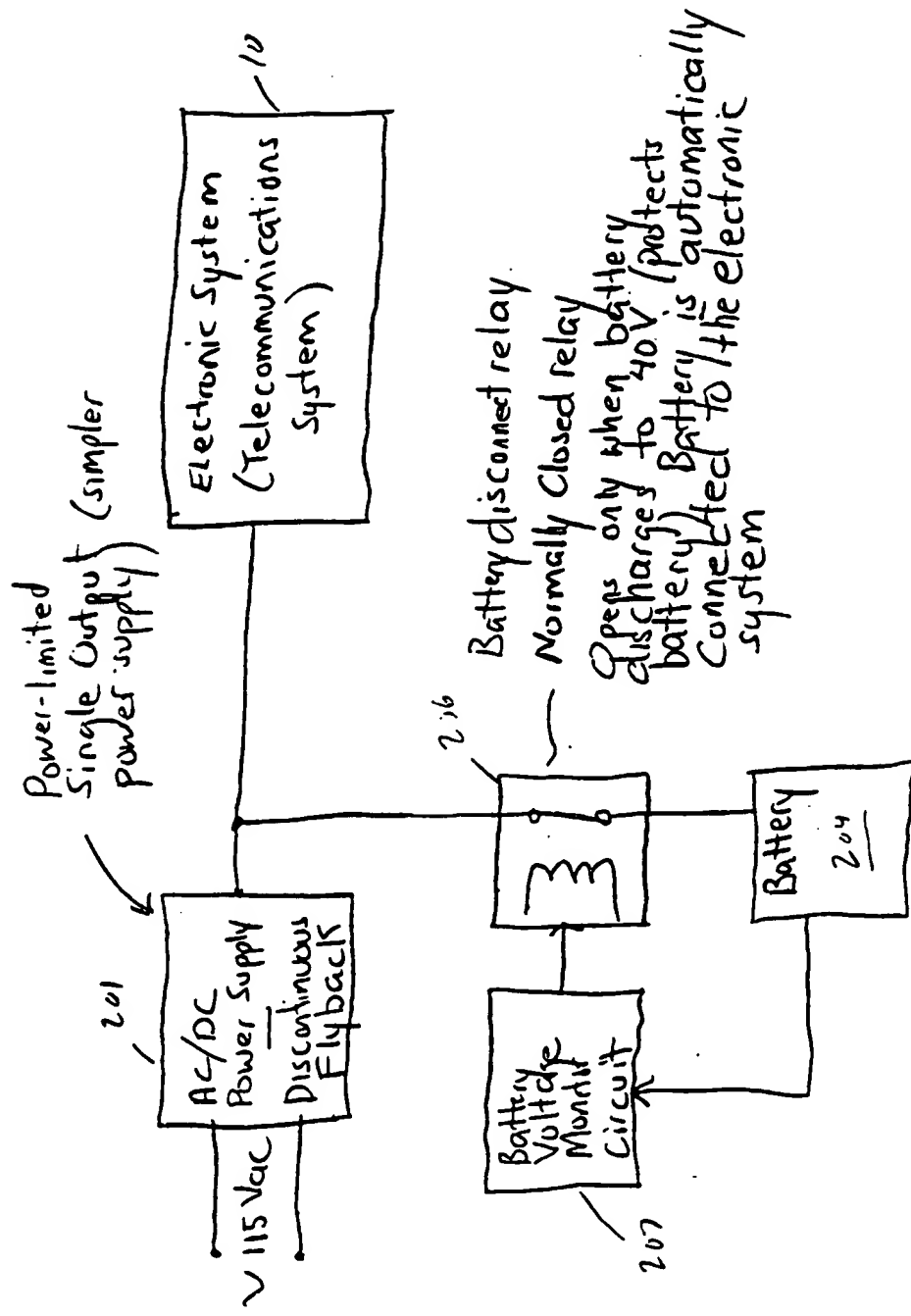


Figure 14 Block Diagram of New Power Supply/Battery Backup System

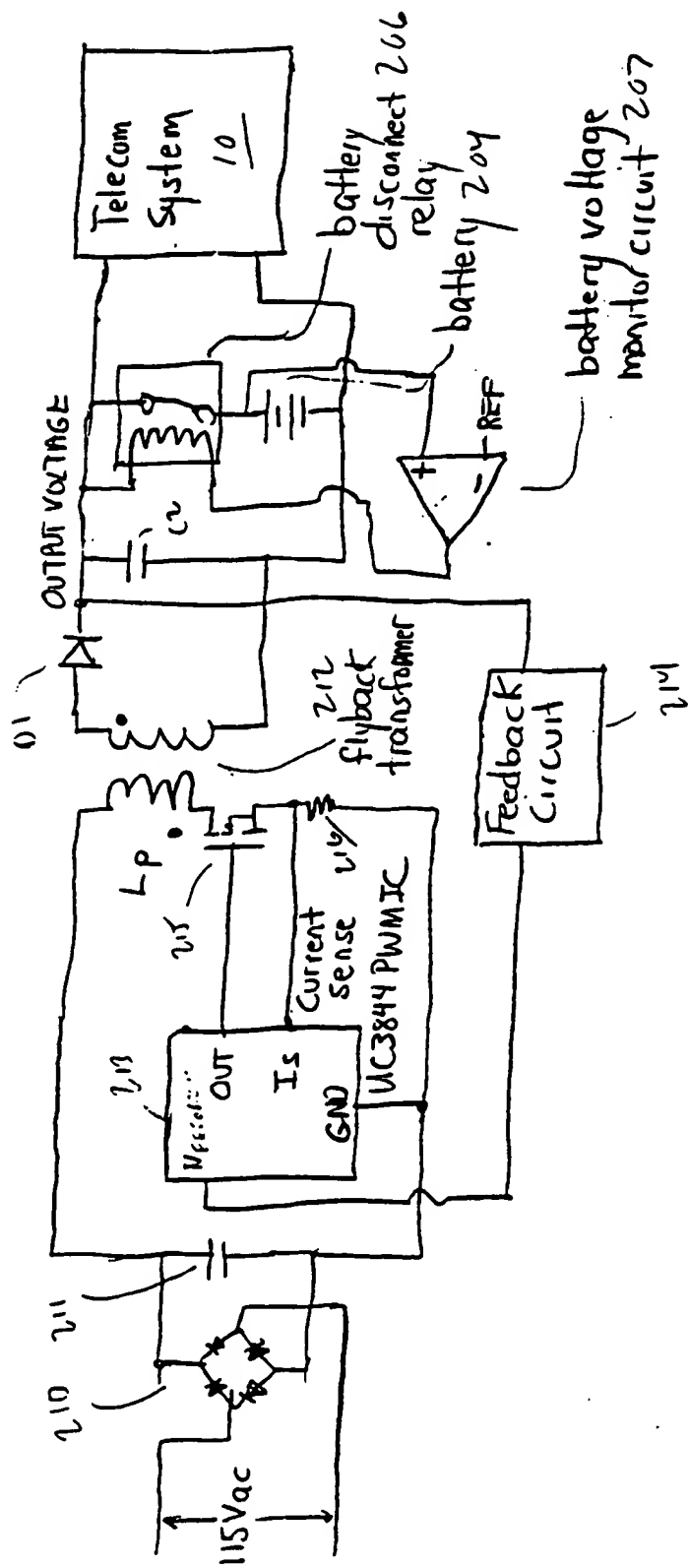


Figure 15- Simplified Schematic of New Power Supply/  
Battery Backup System

~ 200



**Timing Diagram for SPI Receive Status Interface with all Access Modules ( 8 Bits)**  
**Data coming from Access Module**

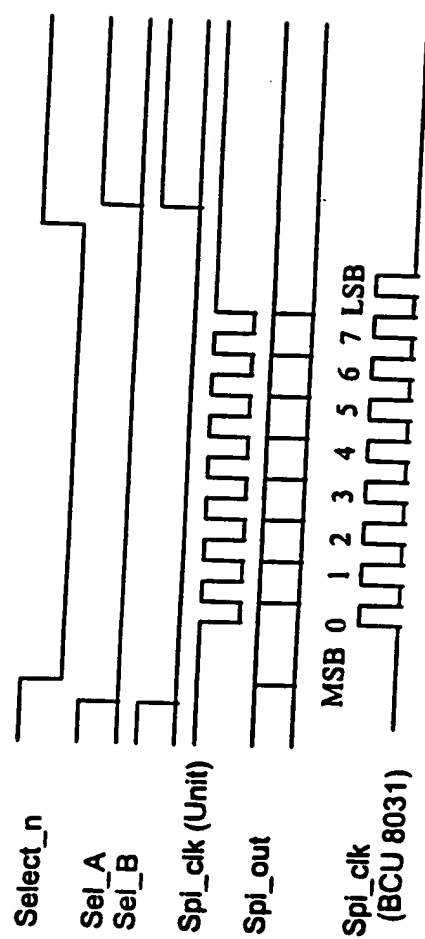


Figure 16

Timing Diagram for SPI Receive Interface from Smart Access Modules for  
Provisioning (9 Bits)  
Data going into Access Module

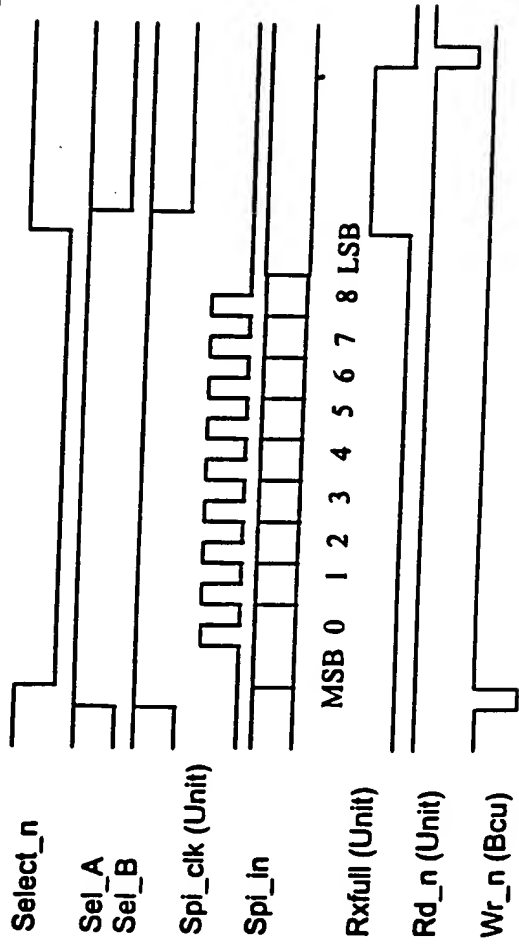


Figure 17

**Timing Diagram for SPI Transmit Interface to Smart Access Modules for Provisioning (9 Bits)**  
**Data coming from Access Module**

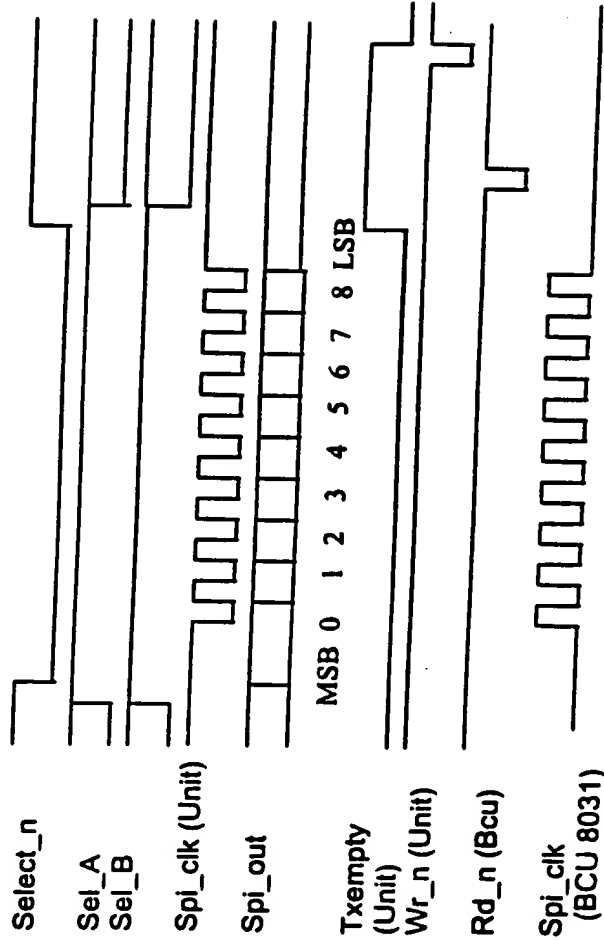


Figure 18

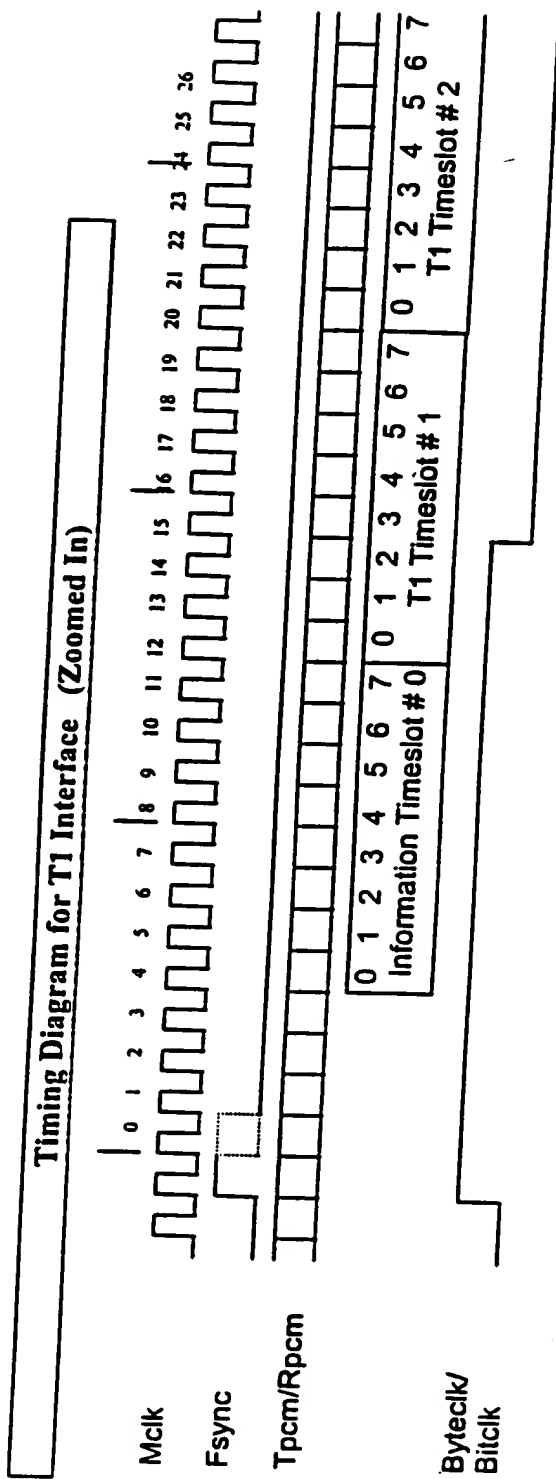


Figure 19



Timing Diagram for T1 Interface (Zoomed Out)

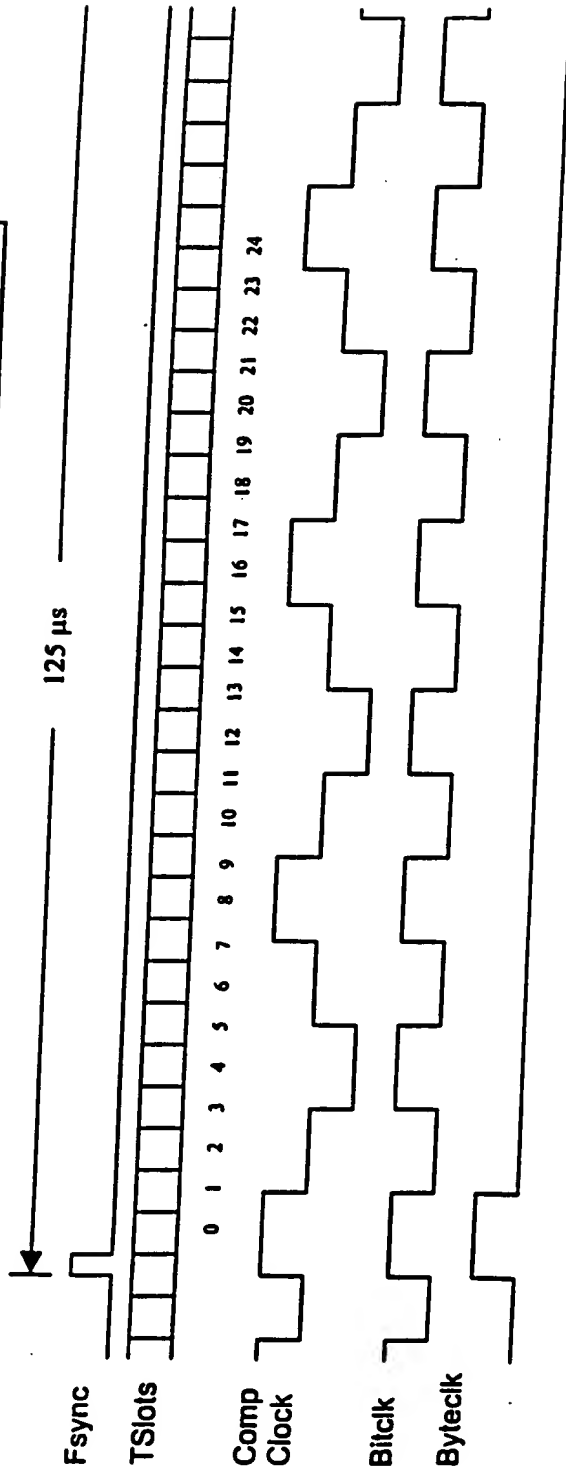


Figure 20